

IRL530N

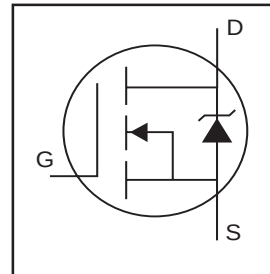
- Logic-Level Gate Drive
- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

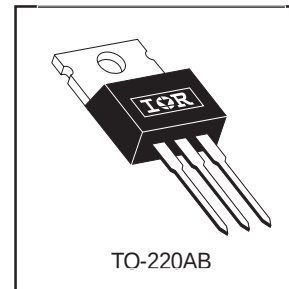
HEXFET® Power MOSFET



$$V_{DS} = 100V$$

$$R_{DS(on)} = 0.10\Omega$$

$$I_D = 17A$$



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	17	A
I_D @ $T_C = 100^\circ C$	Continuous Drain Current, V_{GS} @ 10V	12	
I_{DM}	Pulsed Drain Current ①	60	
P_D @ $T_C = 25^\circ C$	Power Dissipation	79	W
	Linear Derating Factor	0.53	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy②	150	mJ
I_{AR}	Avalanche Current①	9.0	A
E_{AR}	Repetitive Avalanche Energy①	7.9	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

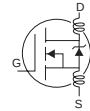
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.9	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

IRL530N

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V$, $I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.122	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.100	Ω	$V_{GS} = 10V$, $I_D = 9.0A$ ④
		—	—	0.120		$V_{GS} = 5.0V$, $I_D = 9.0A$ ④
		—	—	0.150		$V_{GS} = 4.0V$, $I_D = 8.0A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
g_{fs}	Forward Transconductance	7.7	—	—	S	$V_{DS} = 25V$, $I_D = 9.0A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 100V$, $V_{GS} = 0V$
		—	—	250		$V_{DS} = 80V$, $V_{GS} = 0V$, $T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
Q_g	Total Gate Charge	—	—	34	nC	$I_D = 9.0A$
Q_{gs}	Gate-to-Source Charge	—	—	4.8		$V_{DS} = 80V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	20		$V_{GS} = 5.0V$, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	7.2	—	ns	$V_{DD} = 50V$
t_r	Rise Time	—	53	—		$I_D = 9.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	30	—		$R_G = 6.0\Omega$, $V_{GS} = 5.0V$
t_f	Fall Time	—	26	—		$R_D = 5.5\Omega$, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	800	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	160	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	90	—		$f = 1.0MHz$, See Fig. 5



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	17	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	60		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$, $I_S = 9.0A$, $V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	140	210	ns	$T_J = 25^\circ\text{C}$, $I_F = 9.0A$
Q_{rr}	Reverse Recovery Charge	—	740	1100	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 3.1mH$
 $R_G = 25\Omega$, $I_{AS} = 9.0A$. (See Figure 12)

③ $I_{SD} \leq 9.0A$, $di/dt \leq 540A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$

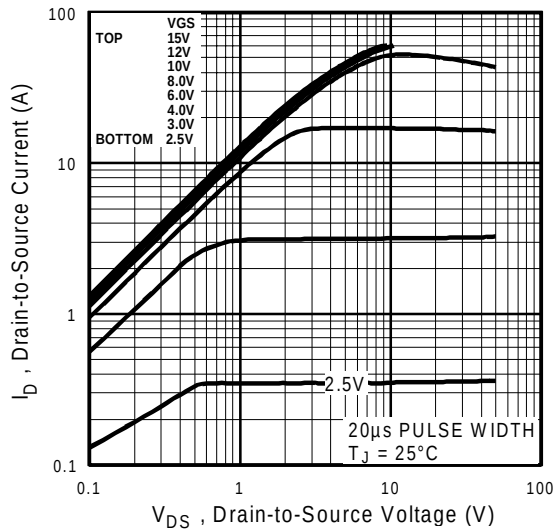


Fig 1. Typical Output Characteristics

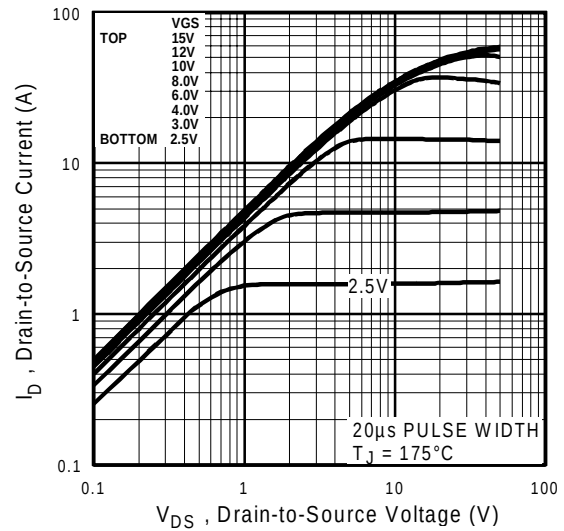


Fig 2. Typical Output Characteristics

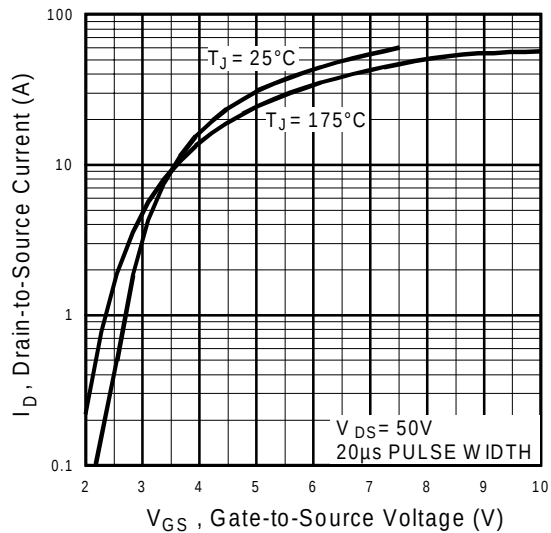


Fig 3. Typical Transfer Characteristics

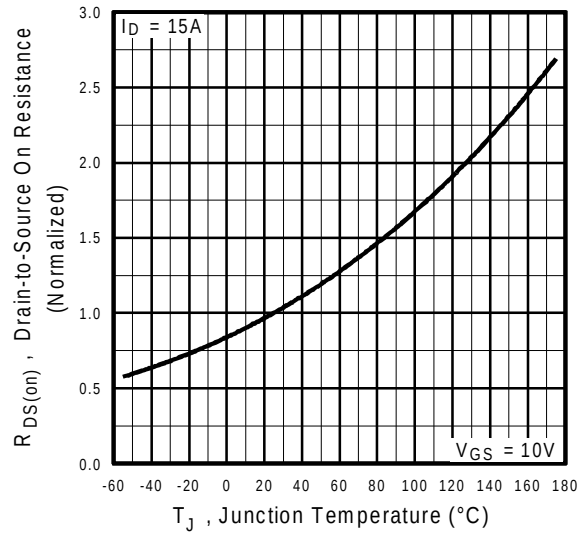


Fig 4. Normalized On-Resistance Vs. Temperature

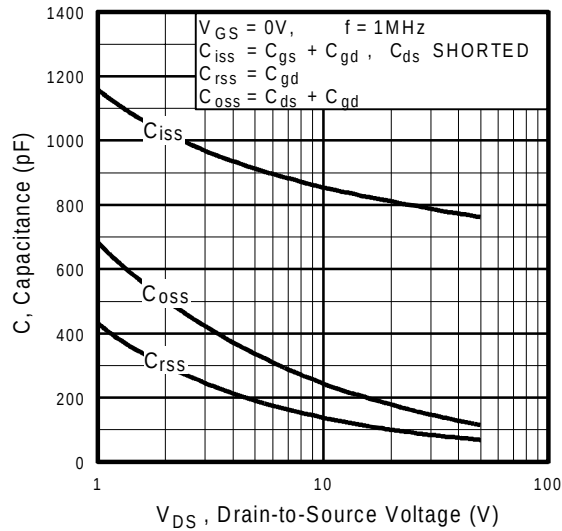


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

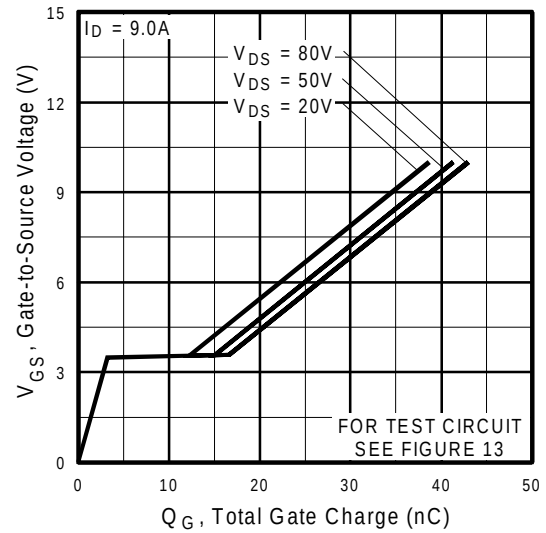


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

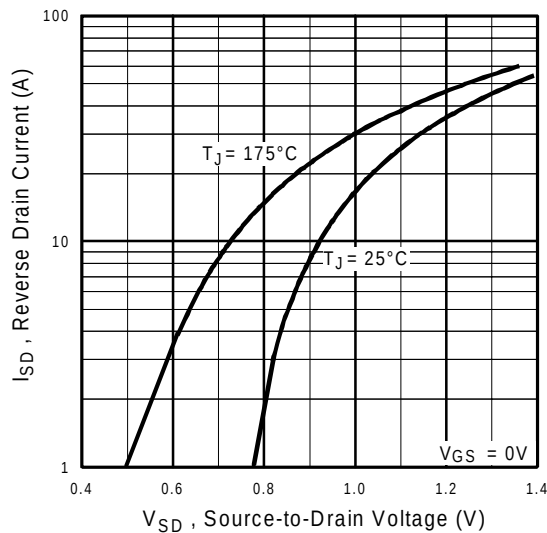


Fig 7. Typical Source-Drain Diode Forward Voltage

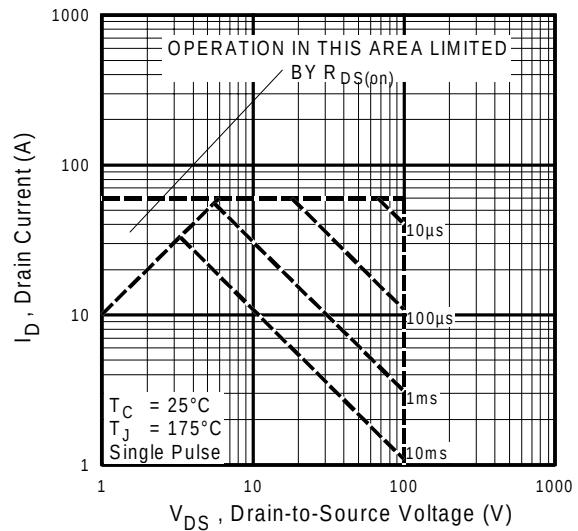


Fig 8. Maximum Safe Operating Area

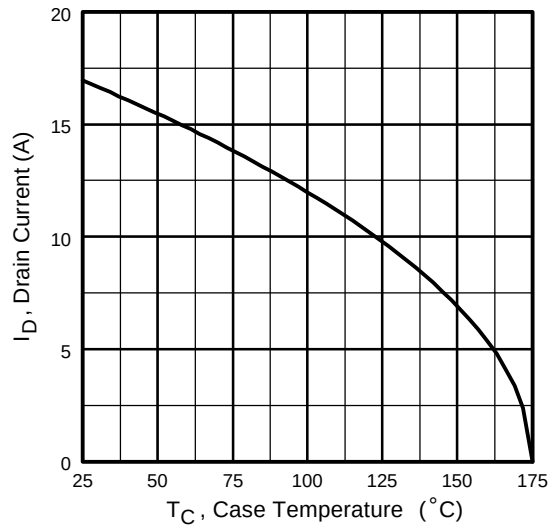


Fig 9. Maximum Drain Current Vs. Case Temperature

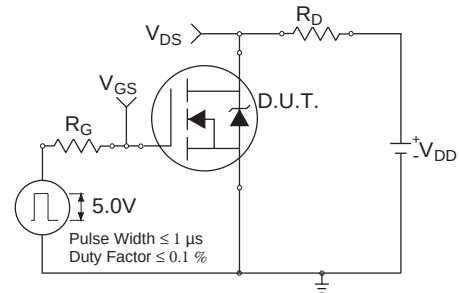


Fig 10a. Switching Time Test Circuit

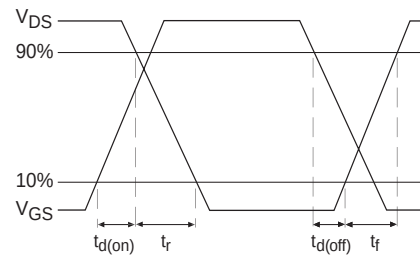


Fig 10b. Switching Time Waveforms

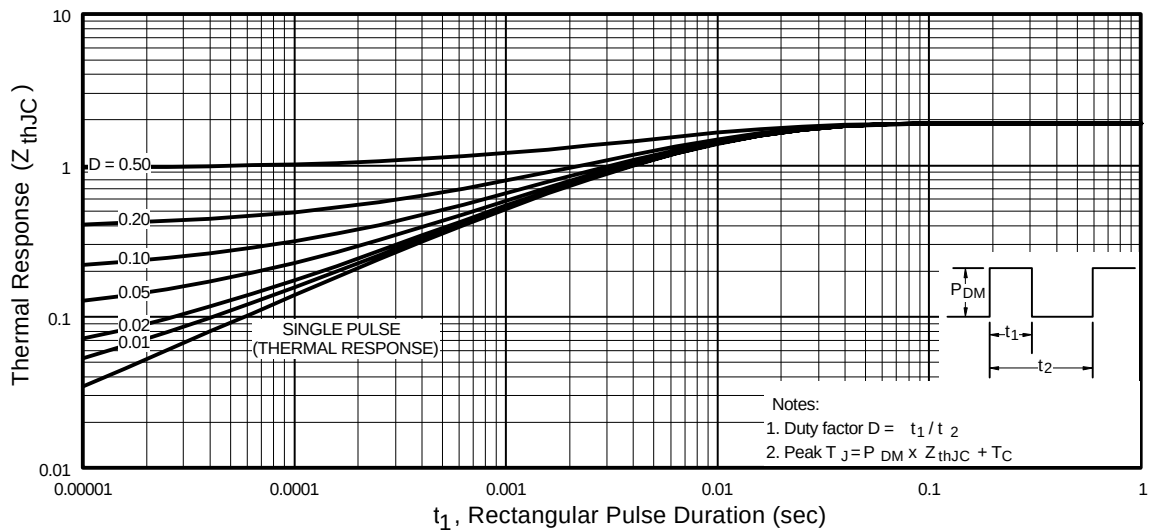


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

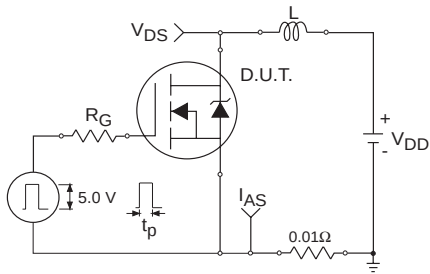


Fig 12a. Unclamped Inductive Test Circuit

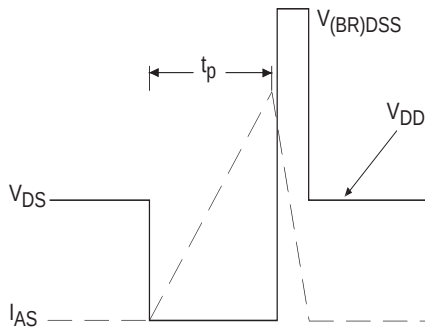


Fig 12b. Unclamped Inductive Waveforms

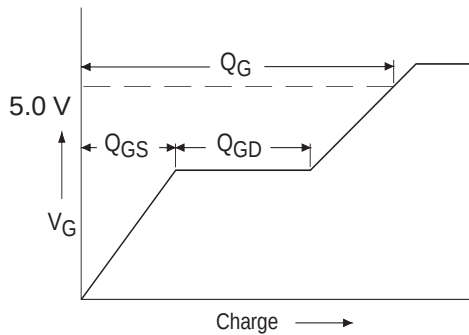


Fig 13a. Basic Gate Charge Waveform

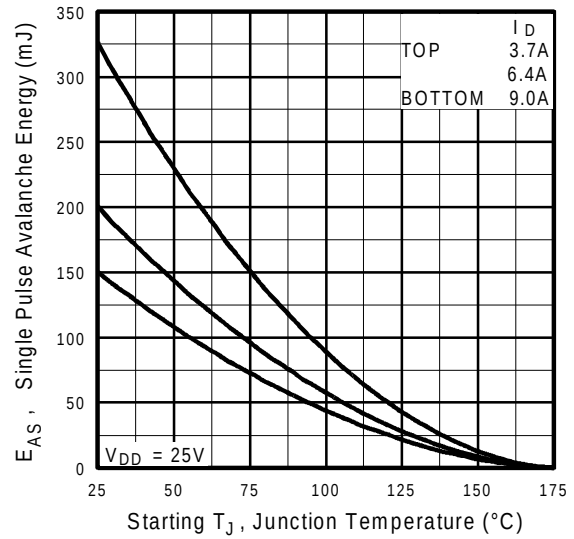


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

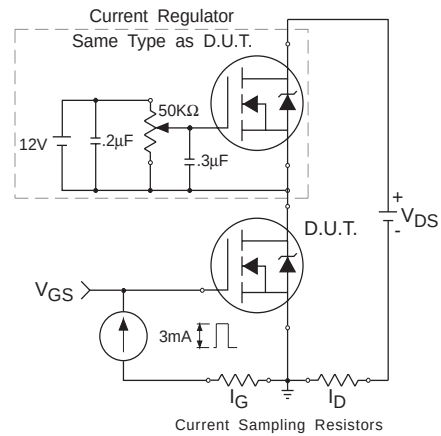
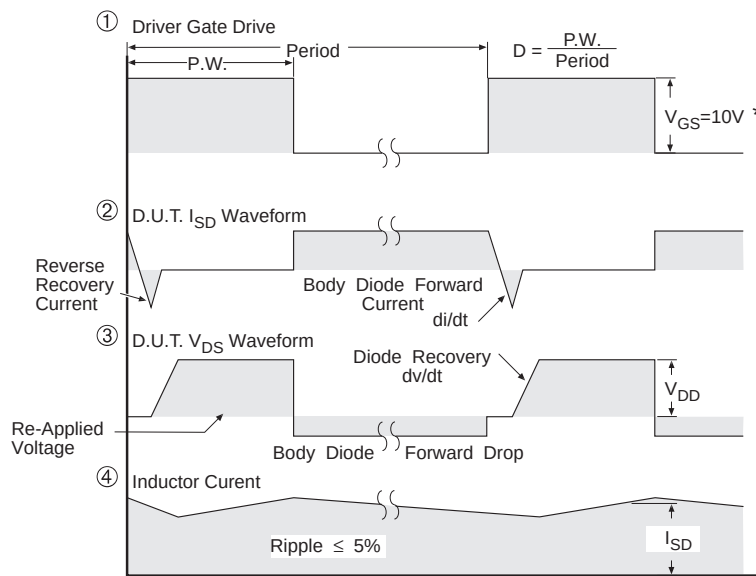
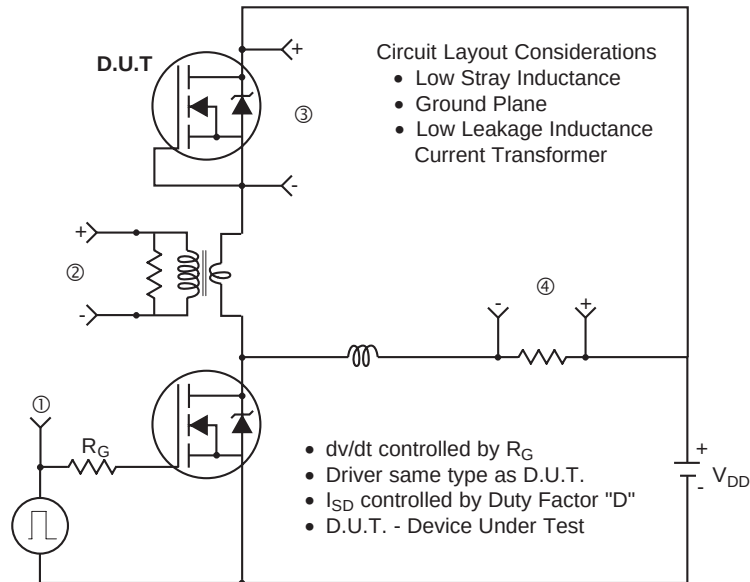


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

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TO-220AB Outline

The drawing consists of two views: a top view on the left and a side view on the right.

Top View Dimensions:

- Overall width: 10.54 (.415) / 10.29 (.405)
- Overall height: 15.24 (.600) / 14.84 (.584)
- Top hole diameter: $\varnothing$ 3.78 (.149) / 3.54 (.139)
- Top hole position: 2.87 (.113) / 2.62 (.103) from left edge; 6.47 (.255) / 6.10 (.240) from top edge.
- Internal hole diameter: 1.15 (.045) MIN
- Internal hole position: 1.40 (.055) / 1.15 (.045) from left edge; 4.06 (.160) / 3.55 (.140) from top edge.
- Bottom hole diameter: $\varnothing$ 0.36 (.014) (M) B A (M)
- Bottom hole position: 1.40 (.055) / 1.15 (.045) from left edge; 2.54 (.100) from bottom edge.
- Lead dimensions: 14.09 (.555) / 13.47 (.530) from top edge; 0.93 (.037) / 0.69 (.027) from bottom edge.

Side View Dimensions:

- Overall height: 4.69 (.185) / 4.20 (.165)
- Lead dimensions: 1.32 (.052) / 1.22 (.048) from top edge; 0.55 (.022) / 0.46 (.018) from bottom edge.
- Bottom hole diameter: 2.92 (.115) / 2.64 (.104)

Lead Assignments:

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE
- 4 - DRAIN

NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB

DATE CODE
(YYWW)
YY = YEAR
WW = WEEK

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